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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
HOGANS, DAVID L	

ART UNIT	PAPER NUMBER
2813	

DATE MAILED: 04/19/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/601,351	CRAFTS, HAROLD S.	
	Examiner	Art Unit	
	David L. Hogans	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *14-30* is/are pending in the application.

4a) Of the above claim(s) *14-19* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *20-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *23 June 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10-31-03, 10-14-03*. +6-23-03
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to the IDS filed on October 31, 2003.

Election/Restrictions

1. Restriction to one of the following inventions is required under 35 U.S.C. 121:

   I. Claims 14-19, drawn to a method of fabricating, classified in class 438, subclass 622.

   II. Claims 20-30, drawn to an integrated circuit, classified in class 257, subclass 369.

The inventions are distinct, each from the other because of the following reasons:

2. Inventions I and II are related as process of making and product made. The inventions are distinct if either or both of the following can be shown: (1) that the process as claimed can be used to make other and materially different product or (2) that the product as claimed can be made by another and materially different process (MPEP § 806.05(f)). In the instant case, the product as claimed can be made by another and materially different process, such as, the process need not utilize a second layer of metallization to connect at least two of said MACRO's.

3. Because these inventions are distinct for the reasons given above and have acquired a separate status in the art as shown by their different classification, restriction for examination purposes as indicated is proper.

4. Because these inventions are distinct for the reasons given above and the search required for Group I is not required for Group II, restriction for examination purposes as indicated is proper.

5. During a telephone conversation with Irvin E. Branch on April 6, 2004, a provisional election was made with traverse to prosecute the invention of Group II, claims 20-30. Affirmation of this election must be made by applicant in replying to this Office action. Claims 14-19 have been withdrawn from further consideration by the examiner, 37 CFR 1.142(b), as being drawn to a non-elected invention.

Status of Claims

Claims 1-13 are cancelled. Claims 20-30 are pending. Claims 14-19 are withdrawn.

Information Disclosure Statement

6. The information disclosure statements (IDS's) submitted on October 31, 2003, October 14, 2003, and June 23, 2003, are in compliance with the provisions of 37 CFR 1.97, and accordingly, have been considered by the examiner.

Drawings

7. The drawings are objected to under 37 CFR 1.83(a) because they fail to show "trace T" in Figure 8 as described in paragraph [52[in the specification. Any structural detail that is essential for a proper understanding of the disclosed invention should be shown in the drawing. MPEP § 608.02(d). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Specification

8. The disclosure is objected to because of the following informalities: the specification fails to teach how the gate and drains of the transistors are formed in the same layer and a second layer of metallization interconnecting a plurality of MACRO's.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

9. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

10. Claims 20-30 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. Claim 20 claims that the gate and drains are formed in the same layer of polysilicon. The Examiner notes that paragraphs 40, 52 and 65 of Applicant's specification most directly address the scope of Claim 20. These paragraphs fail to elucidate wherein how the gate and drain are made from the same layer (i.e. - are the gate and drain etched out of the same layer or are these elements later deposited upon the substrate). The specification appears to provide support for wherein a "connection C between the drains D is fabricated from the same polysilicon layer as the gate G" but fails to provide support for wherein drains D are formed from the same polysilicon layer

as the gate G. The Examiner notes that drains are conventionally located within the wafer of an IGFET.

11. Claims 24-30 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. The specification fails to provide support for the following element of Claim 24: "a second layer of metallization interconnecting said plurality of MACROs."

12. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

13. Claims 20-30 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claim 20 recites a drain of the p-channel field effect transistor and a drain of the n-channel field effect transistor formed in said same layer of polysilicon as the gate. As a field effect transistor can either be a JFET or an IGFET, the Examiner is uncertain as to the location of the drain. For Example, if the field effect transistor is an IGFET, the drain is conventionally located within the substrate (demarcated with numeral 3 in Figure 1). The Examiner would like the Applicant to clarify whether the drains are located above the substrate (demarcated with numeral 3 in Figure 1) or within the substrate?

Claim Rejections - 35 USC § 103

14. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

15. Claims 20 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over 4,482,810 to Cooke in view of 5,168,072 to Moslehi.

Claim 20

Cooke teaches a logic inverter (I1 or I2); an n-channel field effect transistor (10 or 12); a p-channel field effect transistor (10 or 12); and a gate (T1, T2, I1 and I2) formed in a layer of polysilicon. (See Figures 1-4 and columns 4-6 lines 40-50)

Cooke fails to explicitly teach wherein a drain of the p-channel field effect transistor and a drain of the n-channel field effect transistor are formed in said same layer of polysilicon.

However, Moslehi, in Figures 2-19 and columns 5-21 lines 55-17 (noting column 14), teaches wherein the gate (68, 88 or 94) and drain (66, 87 or 92) of a NMOS or PMOS field effect transistor are formed in said same layer of polysilicon.

It would have been obvious to one of ordinary skill in the art to modify Cooke by incorporating wherein the gate and drain of a NMOS or PMOS field effect transistor are

formed in said same layer of polysilicon, as taught by Moslehi, to allow simultaneous doping of drain and gate regions

Claim 21

Incorporating all arguments of Claim 20 and noting that Cooke fails to teach wherein the polysilicon comprising said gate is coplanar with the polysilicon comprising said drain of the p-channel field effect transistor and said drain of the n-channel field effect transistor.

However, Moslehi, in Figures 2-19 and columns 5-21 lines 55-17, teaches wherein the polysilicon comprising said gate (68, 88 or 94) is coplanar with the polysilicon comprising said drain (66, 87 or 92) of the p-channel field effect transistor or said drain (66, 87 or 92) of the n-channel field effect transistor.

It would have been obvious to one of ordinary skill in the art to modify Cooke by incorporating wherein the polysilicon comprising said gate is coplanar with the polysilicon comprising said drain of the p-channel field effect transistor or said drain of the n-channel field effect transistor, as taught by Moslehi, to provide a planar device that will not require numerous back end etch processing steps.

Claim 25

Incorporating all arguments of Claims 20 and 24 and noting that Cooke teaches wherein a trace connects said drain of said p-channel field effect transistor and said drain of said n-channel field effect transistor. (See Figures 1-4 and columns 4-6 lines 40-50)

Although Cooke does not teach forming the trace of polysilicon (i.e. – Cooke teaches the trace comprised of metal), the Examiner notes that it would have been obvious to one of ordinary skill in the art at the time the invention was made to use a silicon based material, since it has been held to be within the general skill of a worker in the art to select a known material based on its suitability for its intended use. *In re Leshin*, 125 USPQ 416 (CCPA 1960)

16. Claims 22-24 and 26-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over 4,482,810 to Cooke in view of 5,168,072 to Moslehi further in view of 3,808,475 to Buelow et al.

Claims 22 and 23

Incorporating all arguments of Claim 20 and noting that Cooke and Moslehi fail to explicitly teach a first layer of metallization and a second layer of metallization, wherein said second layer of metallization comprises no local interconnect.

However, Buelow et al., in column 8 lines 16-53, teaches a first layer of metallization (109) and a second layer of metallization (117), wherein said second layer of metallization comprises no local interconnect.

It would have been obvious to one of ordinary skill in the art to modify Cooke and Moslehi by incorporating a first layer of metallization and a second layer of metallization, wherein said second layer of metallization comprises no local interconnect, as taught by Buelow et al., to obtain a lower voltage drop on the ground bus system.

Claims 24 and 26-28

Incorporating all arguments of Claim 20 and noting that Cooke and Moslehi fail to explicitly teach a plurality of MACRO's, a first layer of metallization and a second layer of metallization interconnecting said plurality of MACRO's, further comprising no local interconnect in said second layer of metallization in all of said MACRO's.

However, Buelow et al., in Figures 4-13 and columns 3-10 lines 40-65, teaches a plurality of MACRO's, a first layer of metallization and a second layer of metallization interconnecting said plurality of MACRO's, further comprising no local interconnect in said second layer of metallization in all of said MACRO's.

It would have been obvious to one of ordinary skill in the art to modify Cooke and Moslehi by incorporating a plurality of MACRO's, a first layer of metallization and a

second layer of metallization interconnecting said plurality of MACRO's, further comprising no local interconnect in said second layer of metallization in all of said MACRO's, as taught by Buelow et al., to obtain a lower voltage drop on the ground bus system.

17. Claims 29-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over 4,482,810 to Cooke in view of 5,168,072 to Moslehi further in view of 3,808,475 to Buelow et al. as applied to claims 20 and 24 above, and further in view of 5,313,079 to Brasen et al.

Claims 29 and 30

Incorporating all arguments of Claims 20 and 24 and noting that Cooke, Moslehi and Buelow et al. fail to incorporate wherein at least one of said MACRO's is comprised by a standard cell array with a common row pitch.

However, Brasen et al., in Figures 3-5 and columns 5-10 lines 01-23, teaches wherein at least one of said MACRO's is comprised by a standard cell array with a common row pitch.

It would have been obvious to one of ordinary skill in the art to modify Cooke, Moslehi and Buelow et al. by incorporating wherein at least one of said MACRO's is

comprised by a standard cell array with a common row pitch, as taught by Brasen et al., to provide flexible routing of routing channels.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to David L. Hogans whose telephone number is (571) 272-1691. The examiner can normally be reached on M-F (7:30-4:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead Jr. can be reached on (571) 272-1702. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

dh DH

Tuan H. Nguyen

Tuan H. Nguyen
Primary Examiner